A universal processor for high speed communication

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Abstract *In up to date digital communication engineering, it is important to use highly flexible hardware units to cope with the rapidly changing demands. This paper presents a special purpose programmable processor architecture, well suited for high speed data communication and multi-carrier signal processing in high-frequency cellular base stations or wide band monitoring applications, where multiple channel operations are required. Due to this intention, several hardware resources are implemented in a complex multi-path pipelined hardware structure controlled by a flexible controller unit. The implemented controller allows high programmability for applications including:*

- *multi channel signal processing,*
- *multi rate processing,*
- *analytic signal processing.*

Finally, standard cell mapping results in a prototype VLSI implementation using Alcatel-Mitec 0.35 μm 5-layer CMOS technology are given.

Keywords: Multichannel Signal Processing, Programmable Pipeline Structure, Digital Audio Broadcast, Beam Forming, Monitor Application

1 Introduction

In digital communication engineering, it is important to use highly programmable and flexible hardware units applicable in various operational areas. In particular for ATM networks, high-speed wireless LANs, ADSL or in Digital Audio Broadcast Systems [1] [2], it becomes more important to handle and control a large quantity of high speed data channels with a small hardware unit.

In these fields, some chip manufacturers like Harris Semiconductors and Qualcomm have developed ASICs for high-speed data communications and digital radio software receivers [9] [11]. These programmable chips perform single-channel signal processing, down conversion, decimation, narrow band low pass filtering, gain scaling and resampling. Furthermore these chips provide the direct demodulation of ASK, FSK, PSK for single channel application. Other types of their ASICs handle up to four independently programmable data channels with fixed or floating point arithmetic without on chip demodulation units [10].

All these special purpose devices referenced above have the following properties:

- they are not highly programmable for a wide range of applications and
- they are not easily expandable to control a couple of data channels.

Analyzing these chips, their architectures contain processing units for a specific number of data channels in parallel. Thus, the architectures mentioned above need a lot of silicon area per channel. Price and power usage increases. This is not acceptable for small and cheap devices e.g. for high speed mobile communications.

Alternative architectures proposed in the literature are stand alone ASIC's for wireless data communications [8] or reconfigurable hardware structures with a fixed number of processing elements [6] [7].

The major outstanding feature of our realized processor architecture is the high degree of programmability with the implemented resource units to handle numerous high speed data channels by Time-Division Multiple Access (TDMA). For this intention, we use a multi function multi-path pipeline architecture in combination with a fast controller unit [3].

The realized prototype chip directly processes digital samples from a high speed A/D converter [12] [13]. The processor may operate as a preprocessing hardware circuit. After the preprocessing task, slower units like a conventional DSP or standard micro-controller may process data arbitration or evaluation tasks.

The outline of the paper is as follows: In the next section, we introduce and discuss our processor architecture concept and focus on high programmability and flexibility to handle numerous data channels. In section 3, we present the processor architecture and the implemented resource units. Section 4 treats the programmable concepts and gives an example of a successive decimation of a bandpass signal. Results for a prototype realization in Alcatel-Mitec 0.35 μm 5-layer CMOS technology are given in section 5, while some concluding remarks are given in section 6.

2 Architecture Concepts

The processor architecture consists of resource units, which will be typical used in high speed communication environments. Due to the need of fast digital filtering for most of the operational areas, we dispose massive parallel FIR-filter pipes in direct form realization. To minimize the cost of digital parallel FIR-filter structures on chip, we implement a special filter structure which utilizes the symmetric properties of linear phase filter coefficients. A cascade of separate FIR-filter pipes with common multipliers is implemented respectively in a Real- and Imaginary Filter Block.

A major feature of the realized hardware structure is the analytic signal processing to attain the whole channel bandwidth. For this purpose, a complex multiplier and a quadrature NCO (Numerical Controlled Oscillator) resource are programmable to maintain a quadrature mixer structure. After the conversion, the real and imaginary components of the complex signal are processed separately.

The implemented resource units can be used by TDMA. Therefore, the controller unit manages the resources via a simple infinite program loop of up to 16 instructions without branches. Supplementarily, the processor architecture allows data feedbacks. The program of the processing sequence and the filter coefficients for an application can be loaded. We use only FIR-filter pipeline registers and a coefficient bank memory on chip. Thus, the data flow architecture is predominantly constructed for real time applications without sample data buffering. With a dedicated communication port, the chip can communicate with external hardware. For processor configuration, a special serial port is provided.

3 Processor Architecture

Figure 1 depicts the overall architecture of the realized processor architecture. It consists of a Real- and Imaginary Filter Block to calculate the real and imaginary parts of an analytic signal, a quadrature NCO and a complex multiplier which is interconnected to the filter block inputs. The four multiplexer (MUX) controls the complex multiplier hardware resource for individual use. To maintain a quadrature mixer structure, a constant multiplier value of 0 disables the unused hardware multiplier. A multiplication with the complex constant 1 lets the sample data pass through. For shifting the analytic signal in the frequency domain, the complex multiplier resource uses the NCO quadrature signal. Two multiplexers (Data-MUX) for each of the real- and imaginary parts control sample data streams as feedback from the filter blocks or new input samples from the A/D converter. Additionally, two multiplexers (OutMUX) may optionally distribute calculated sample data from various filter pipes inside the filter blocks to other hardware units outside the chip.

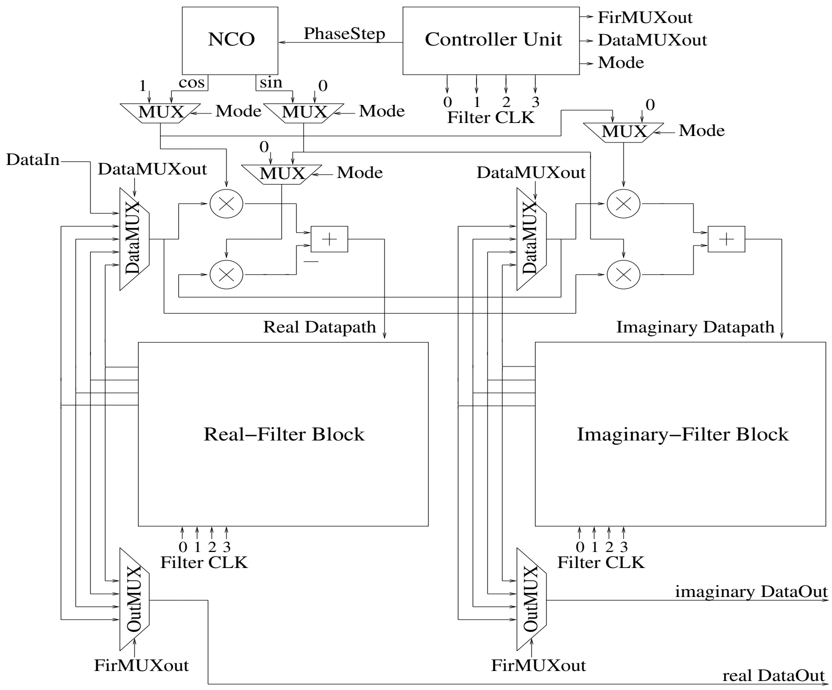

Figure 1: Structure and wiring scheme of the processor organization with the implemented hardware resource units.

The implemented controller unit manages the pipeline execution flow by configuring the implemented hardware resources in every time slot via dedicated control wires. This results in a programmable multi-path pipeline hardware structure. In the following, we specify the implemented resource units.

3.1 Quadrature NCO

The quadrature NCO hardware can be used in TDMA to realize up to four independent NCO's by providing four 32-bit phase accumulators and four phase step registers.

3.2 Complex Multiplier

The complex multiplication resource unit involves four separate multipliers and two adder components. Its input is selected by four input multiplexers (MUX) and it may be changed in every cycle. The complex multiplier is usable for a desired number of data channels.

We can differentiate three major processor functionalities which are controlled by the global controller unit:

- Converting a real input signal into a complex one by configuring the implemented complex multiplier hardware structure and the quadrature NCO as quadrature mixer structure.
- Complex processing of the sample data by performing the complex multiplication in hardware.
- Frequency shifting by complex multiplication using the quadrature NCO signal.

The complex multiplier outputs are directly connected to the Real- and Imaginary Filter Blocks.

3.3 Real- and Imaginary Filter Block

The chip contains two identical filter blocks with a structure shown in Figure 2. A filter block consists of parallel FIR-filter pipe resources in direct form with odd numbers of

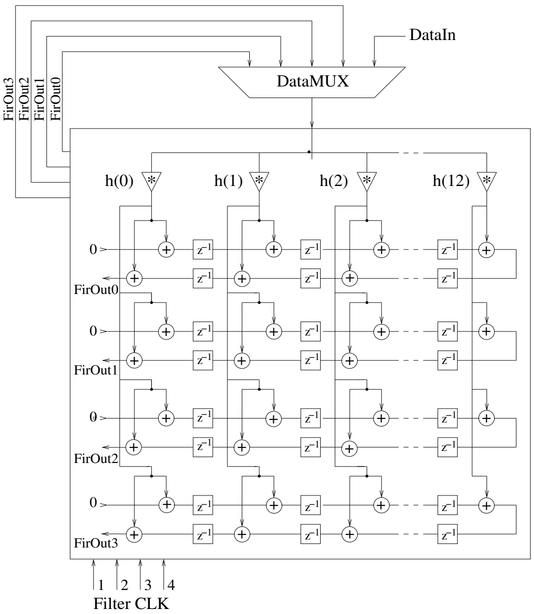

Figure 2: Architecture overview of a FIR-filter block structure with the independent FIR-filters pipes, global multiplier for each partition filter, the coefficient registers h(0) to h(12) and the feedback multiplexer (DataMUX). The first adder in every filter pipe is not realized. The complex multiplication part were omitted for clarity.

FIR-filter coefficients. The implemented FIR-filter resource efficiently exploits the symmetric properties of the linear phase FIR-filter coefficients. Due to this, there are effective 25 filter coefficients for each FIR-filter pipe realized with 13 coefficient registers.

The FIR-filters use the same set of multipliers, but selectable filter coefficients from the filter coefficient bank. At any time only one of these four FIR-filters is selected. The filter coefficient bank in the prototype chip stores 52 filter coefficients of 14 bits each. Due to the lack of on-chip data buffer, the number of controlled data channels is restricted to the number of FIR-filter pipes. The filter blocks allows high speed multichannel complex filtering. If real filtering is desired, each filter block can operate separately.

4 Programmability and Flexibility

The controller unit of the prototype chip is realized as a simple sixteen-step finite state machine (FSM) which runs synchronously to the specified sample rate clock.

4.1 Program Example

To demonstrate programmability and flexibility, we illustrate an example: Starting from the implemented controller unit with up to sixteen instructions, we have an equivalent number of usable reservation time slots. The allocation of these time slots can be freely predefined by the user via a determined programming sequence. The sequence may consists of several micro instructions. The micro instructions directly depict the register of the hardware register and control wires.

For a simple program example, we realize a successive decimation by two for a bandpass signal. Figure 3 illustrates the required programming sequence. The sixteenth time slot transfers the decimation result to the output port via the output multiplexer. Figure 4 illustrates the decimation in the frequency domain.

TimeSlot:	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19
Fir–Filter1	*		*		*		*		*		*		*		*		*		*
Fir–Filter2		*				*				*				*				*	
Fir–Filter3				*								*							
Fir–Filter4								*											

Figure 3: Reservation table of a decimation by sixteen using four decimation steps of 2. A star (*) in time slot k means computation of the selected FIR-filter. The processing period is 16, indicated by the vertical dashed line.

For the same decimation factor in every FIR-filter stage, the sample rate after k decimation stages is

$$f_d = \frac{f_s}{d^k} \tag{1}$$

with f_s being the sample frequencies and d the decimation factor. Due to the realized six-

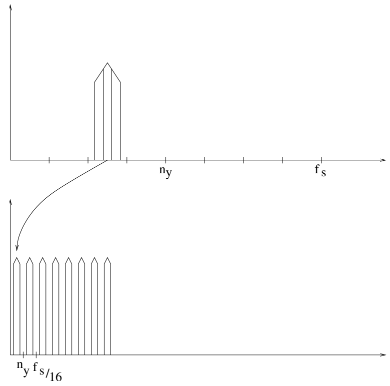

Figure 4: Decimation example by sixteen disposed on an conventional band path signal in the frequency domain.

teen step pipeline flow and the fact that there are four independent FIR-filter pipes in each filter block, the maximum decimation factor is $16^4 = 65536$.

5 VLSI Implementation

The prototype chip integrates four independent FIR-filter pipes in direct form with global multipliers in each filter block. The number of FIR-filter coefficient registers is thirteen for each partition FIR-filter pipe. For the proposed applications, we use in our prototype design 14-bit data paths for samples and filter coefficients to get a maximum of 84 dB signal-noise ratio. The complex output from the quadrature NCO is 14-bit. There are four 32-bit phase accumulator register implemented. All arithmetic components use fix-point precision.

The hardware model was programmed in VHDL under a Solaris system on a workstation platform. All components of the chip have been simulated with VHDL System-Simulator (VSS) [14]. After complete verification of the design functionality, it was then synthesized using appropriate timing constraints with the Synopsys Design Compiler (DC). The chip has been mapped using an Alcatel-Mitec 0.35 μm 5-layer CMOS target process optimized for a 3.3V supply voltage. The final layout shown in figure 5 has a total area of 8,91 mm^2 including 87 pads. A filter block will use 3.56 mm^2 silicon area. The number of standard cells is 38180. It is a core-limited design due to EUROCHIP bonding restrictions. For placement and routing, the silicon ensemble tool was used. After a layout timing analysis via Cadence Leapfrog [15], the chip is fully functional at clock frequencies up to 160 MHz. The critical timing path will go through the adder and the booth-encoded multiplier of the complex hardware structure. Due to the analytic signal processing, the maximum working bandwidth is 160 MHz.

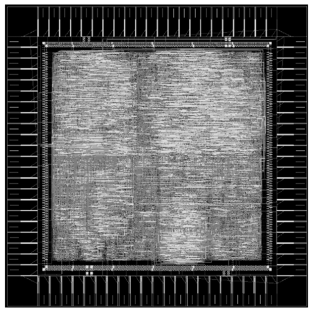

Figure 5: Layout of the prototype chip realization. For the maximum clock speed there are no conventional ram blocks for the coefficients implemented. The registers for the coefficients are directly integrated in the logic.

6 Conclusion

A universally applicable processor for high speed data communication, multi-carrier signal processing in high-frequency cellular base stations or monitoring applications has been presented. The architecture was developed to control a variable number of independent high speed data channels. The processor structure provides massive parallel FIR-filter pipes, a complex multiplier and a programmable quadrature NCO which can be used for conversion, channel selection and carrier tracking. We described the functionality of the realized filter blocks and the linear phase FIR-filter structures, the analytic signal processing and three major processor functionalities. In our hardware implementation, we use a programmable multi-path pipeline structure controlled by an implemented controller unit via a small set of micro instructions. The controller unit manage the multi-path pipeline execution flow towards a dedicated time slot reservation table.

A small proof-of-concept prototype chip with 14-bit data paths and a filter bank of 52 filter coefficients for the implemented FIR-filter pipes has been developed using the Alcatel-Mitec 0.35 μm 5-layer CMOS process. The chip provides a parallel working communication port to transfer sample data to other hardware units in real and imaginary parts separately. An implemented serial port configures the controller unit and the required FIR-filter coefficient bank for various applications.

We see the operational area of the proposed processor architecture principally as an IP-core (Intellectual-Property) in an SOC (System-on-Chip) or as stand alone chip in fast digital communication environments or in upcoming bluetooth solutions, where numerous data channels must be controlled. Another operational area can be emergency monitoring applications in sea-navigation of wide frequency domains. The processor architecture may also be used for beam-forming [4] [5] or in UMTS environments. The proposed processor hardware architecture is particularly applicable without major expenditure for the suggested applications.

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