An EPLD Based Transient Recorder for Simulation of Video Signal Processing Devices in a VHDL Environment Close to System Level Conditions

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Abstract. An EPLD based low cost transient recorder of video signal bandwidth (sampling rate $25MHz$) is presented. It will be used to record and replay video signals. These video signals are handled by a video processing unit, under construction in a VHDL environment. The main advantage of this self made transient recorder is that the video signal processing device, which is under construction in a VHDL environment, uses the same analog components as the EPLD based transient recorder. Thus, the video signal passes the same signal path and components in the final device. This results in a simulation environment very close to the final system environment.

1 Introduction

The speed of EPLDs available now allow applications in the area of video signal processing. As in the present case, the integration density of current EPLDs allows one to build a low cost transient recorder with few EPLDs and a handful of other components. The relative low effort in realizing a prototype caused by using EPLDs justifies building an EPLD based transient recorder to support simulation in a VHDL environment very close to system level conditions where signals pass through the same components (fig. 1). In the present case this is the exchange of analog video signals with an Flash-ADC and a Video-DAC.

2 Developing Environment and Design Flow

VHDL is used to describe the EPLD designs. The Synopsys VHDL system simulator VSS (Version 3.3) [1] is used for functional simulation of the EPLD designs. The Altera Max+Plus II (Version 5.3) developing system [2] is used to map the VHDL designs to Altera EPLDs [3]. The conception of the architecture was done top-down, but the implementation with VHDL was done bottom-up. Sub-designs were tested stand-alone by functional VHDL simulations before instanced in other sub-designs. During the implementation and functional simulations of the EPLD designs, mapping of sub-designs and determinations of

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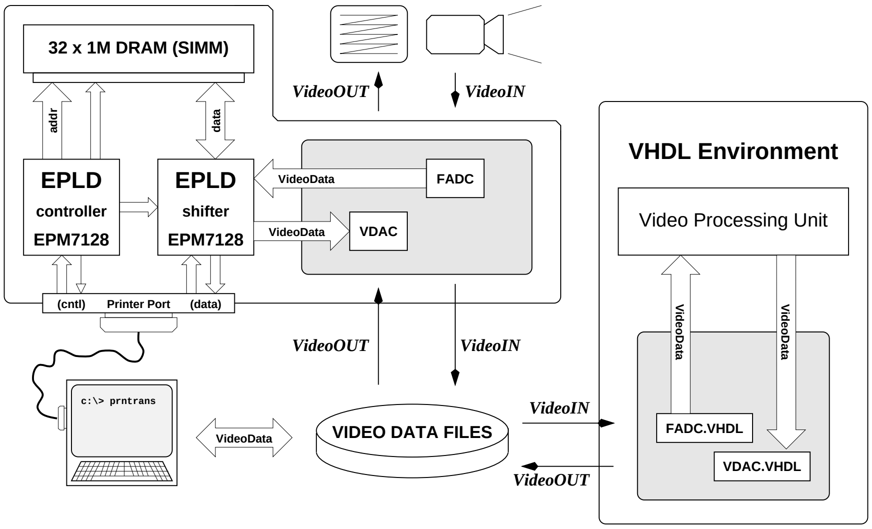

Fig. 1. Signal Flow

resulting speed have been done in accompaniment with the Altera Max+Plus II developing system. This is very important to prevent the impossibility of fitting the final designs with the required speed. System components (FADC, VDAC, parallel printer port) of the transient recorder were implemented as simplified behavioral VHDL models during the development of the transient recorder itself, to support system level simulation. The VHDL models of these components communicate with the control program (equipped with data exchange features beyond the hardware control) of the transient recorder via file read and file write.

3 System Description

The transient recorder consists of an 8 bit FADC (Motorola MC10319 Flash-ADC [4]), a 3×8 bit VDAC (Brooktree Bt121 Video-DAC [5]), DRAM ($4 \times 1M$ Byte SIMMs) and two EPLDs (Altera EPM7128LC84-12 [3]). These two EPLDs (2) implement the whole digital processing of the transient recorder. One of these EPLDs (shifter) implements a 4×8 bit wide video shift register with 25 MHz shift frequency and an additional 4 byte wide data buffer as well (fig. 3). The shift register and buffer register are also used for slow read and write access by a PC via the parallel printer port. The other EPLD (`controller`) performs DRAM control, interfacing with the printer port and generation of the signals to control the data flow of the shift register and buffer register of the shifter EPLD (fig. 4). A video operational amplifier (élantec EL4393C video operational amplifier [7]) is the output buffer which drives a 75Ω video cable.

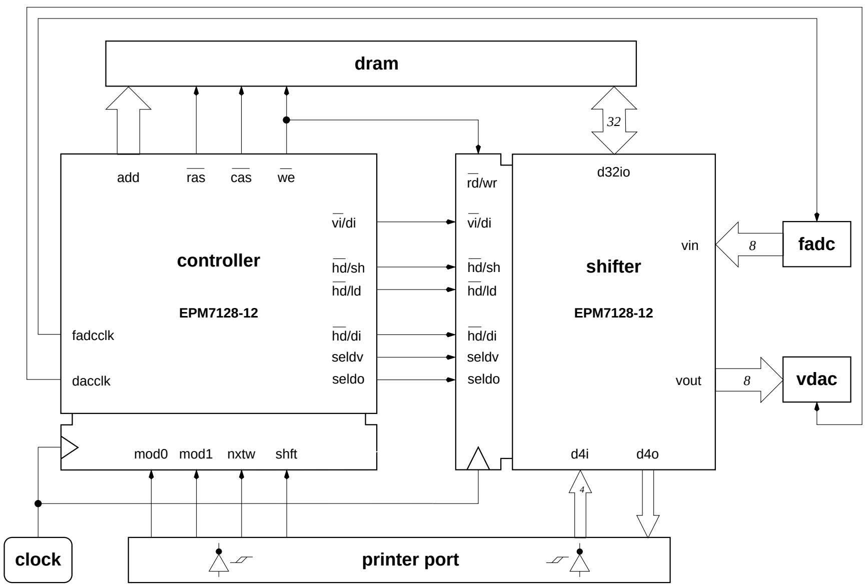

Fig. 2. Controller and Shifter

3.1 Shifter EPLD

The video data stream sampled by the FADC is shifted continuously through a chain of four 8 bit registers. The contents of these four registers can be copied into the 32 bit wide buffer register. The four 8 bit video shift registers can be loaded 32 bit wide in parallel from the DRAMs as well. This allows read and write access to the video shift registers via a 32 bit bidirectional data bus with a quarter of the video shift frequency. An additional 4 bit data input (d4in) and a 4 bit data output (d4out) port allows simple printer port interfacing (fig. 3).

3.2 Controller EPLD

The communication between transient recorder and PC via the printer port [6] is handled by a FSM (cntlfsm (32 states)) of the controller EPLD (fig. 4) which also controls the shifter EPLD (fig. 3). Four operational modes are defined for the transient recorder. The operational mode is selected with two signal lines (called m1 and m0) connected with the printer port. In *record mode* (sample) the digitized data stream coming from the FADC is fed through the video signal register chain to the VDAC. On every fourth shift clock cycle the contents of these registers is copied into the 32 bit buffer register and a DRAM write sequence is forced. DRAM access (refresh and address multiplexing as well) is handled by a sub-controller (dramcntl, dramfsm (9 states)) which is part of the controller

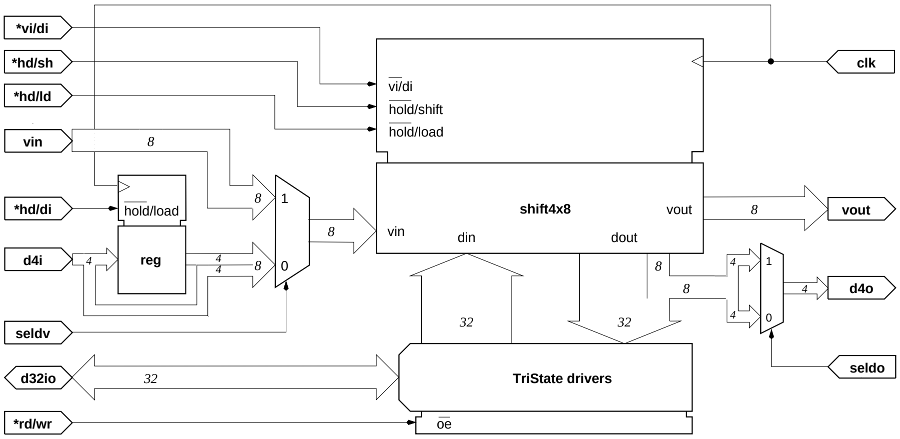

Fig. 3. Video Shifter FPGA

EPLD (fig. 4). In *replay mode* (play) data is read from memory and copied into the video shift register and shifted out similarly to *record mode*. Both, recording and replaying are cyclic with respect to memory addresses.

In *memory read mode* (read) the video shift register has the task of slowly shifting out data read from DRAM to the printer port a half byte wide nibble by nibble. In *memory write mode* (write) the video shift register has the task to shift in nibble by nibble from the printer port similar to the *memory read mode*. Shift and address counter increment is controlled by two additional signal line (called shft and *nxtw*). The control signals (m1, m0, shft, nxtw) are synchronized (invsync) with system clock signal.

3.3 Behavioral Components

A functional VHDL model of the FADC reads sampled video data from a text file (library `ieee`, package `std.textio.all` via `readline(infile,inline)` and `read(inline, sample)` statements). These data can be processed by simulation as if coming from an FADC. Resulting data of simulation can be entered to a functional VHDL model of a DAC which writes these data to a text file via `write(outline,sample)` and `writeline(outfile,outline)` statements. The behavioral VHDL models of FADC, VDAC, and printer port have been used during the development of the EPLD based transient recorder to support it.

4 Results

Both, controller EPLD and shifter EPLD are of type Altera EPM7128LC84-12. This type of EPLD has a functionality of 2500 usable gates [3]. The whole

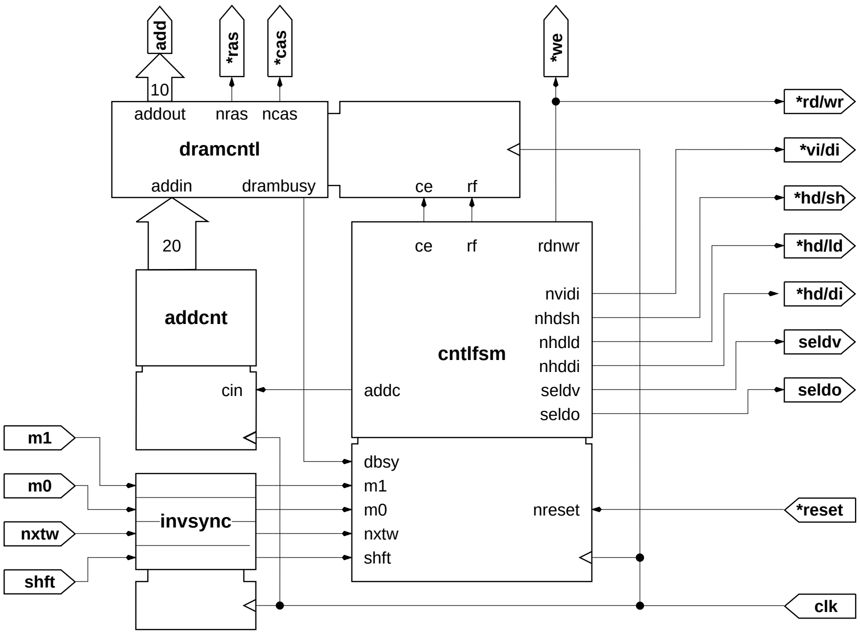

Fig. 4. Controller FPGA

design (controller and shifter) enfolds ≈ 1500 lines of VHDL including behavioral models for system level simulation. The clock frequency of the EPLDs must be twice the requested sampling rate of the FADC. The controller EPLD is utilized by 83% (107 LogicCells, 34 Shareable Expanders) at a maximum clock frequency of 55 MHz. The fitting (controller EPLD) was very sensible with respect to state coding and output coding scheme of the FSM (cntlfsm). The shifter EPLD (EPM7128LC84-12) is utilized by 85% (109 LogicCells, 0 Shareable Expanders) at a maximum clock frequency of $90 MHz$.

References

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