Interfacing Between the 1394a Links and TSB41BA3

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ABSTRACT

The TSB41BA3, a 1394b PHY, can interface to 1394-1995 and 1394a link-layer controllers (LLC) like the following: TSB12LV21B, TSB12LV26, TSB12LV32, TSB42AA4, TSB42AB4, or TSB12LV01B. For integrated 1394 link and PHY such as TSB43AA82A, it can also be connected cable port to cable port. This application report describes overall electrical connections between a Texas Instruments (TI) discrete 1394-1995, 1394a link and TSB41BA3, using the TSB12LV32 and TSB12LV01B as the examples.

Contents

Tables

Terminology

In this application report, several terms are used to describe components of a node-to-node 1394 connections. These terms are defined here to enhance clarity:

Port: refers to the port terminal pins on the PHY device. TSB41BA3 is a three-port PHY device.

Connector: refers to the physical receptacle located in close proximity to the PHY. Its pins are connected directly to the port through the termination resistor networks. The connector is designed to receive a cable's plug.

Plug: located at each end of a 1394 cable and is inserted into the connector.

Cable Interface

The TSB41BA3 cable interface can follow either the 1394a-2000 (1394a) protocol or the 1394b-2002 (1394b) protocol on each port. The mode of operation of any given port is determined by the interface capabilities of the port being connected and the way the port has been configured using the six selection pins (Table 1 of the TSB41BA3 data manual). When any of three ports configured as 1394b bilingual or 1394a data-strobe is connected to a 1394a compliant node, the cable interface of that port operates in the 1394a data-strobe mode at s100, s200, and s400 speed. When any of three ports configured as 1394b beta-only 200 (B2), for example, is connected to a 1394b compliant node, the cable interface of that port operates in the 1394b mode at s100B and s200B speed only.

The 1394b specification extends the 1394 bus speed to s800, s1600, and s3200. A new Beta connector and its associated cable are defined in the 1394b specification. A node that only runs in Beta mode should use the Beta-only connector and Beta cable. For 1394-1995 and 1394a legacy connection, a cable with a legacy plug on one side and a bilingual plug on the other side should be used. A Beta-only or a bilingual PHY port cannot be connected to either the 1394a 4-pin connector or the 1394a 6-pin connector. Only a port that is configured as a 1394a data-strobe port can be connected to either the 1394a 6-pin or the 4-pin connector. Table 1 illustrates the TSB41BA3 connection scheme.

Table 1. Possible Cable Connections

Plug 1	Plug 2	Max Speed
Bilingual	6 Pin Cable (Carries Power)	S400
Bilingual	4 Pin Cable (No Power)	S400
Bilingual	Bilingual	S400B
Beta	Beta	S400B
Beta	Bilingual	S400B

Note: A bilingual plug can not be plugged into a Beta connector.

The port configuration is done through the S5_LINKON, S4, S3, S2_PC0, S1_PC1, and S0_PC2 selection pins. On hardware reset, S5_LINKON, S4, S3, S2_PC0, S1_PC1, and S2_PC2 are selection pins that configure the speed and mode of the ports of the TSB41BA3. Please refer to Table 1 of the TSB41BA3 data manual (SLLS155) for a complete description of the port configuration process.

The cable interface is shown on sheet 1 of the 1394a Link/TSB41BA3 schematic (Appendix A). It includes two 1394b Bilingual Connectors (Connector 0 and Connector 1) that connect to the PHY. Port 2 is not brought out to a connector. Port 2 is an unused port configured as a 1394a port. In this case, mode #2 is used for port configuration; S5_LINKON and S4 are tied to the GND through a 1-kΩ resistor respectively. S3 is tied to DVDD(3.3) through a 1-kΩ resistor. TSB41BA3 automatically determines the correct cable interface connection method for the bilingual ports.

The cable power from each cable is connected to the other ports and is available as bus power. The PHY operates off bus power in the schematic. A voltage regulator regulates the bus power to 3.3V. To be 1394 compliant, the regulator must allow input voltage ranges between 8-V DC and 30-V DC. The voltage regulator is shown on sheet 1 of the 1394a Link/TSB41BA3 schematic (Appendix A). When cable power is not active, the voltage regulator may also be powered from a 12-V source, such as a PC power supply. A diode determines which power source is used. For protection, a 0.75-A fuse should be used in-line with the 12-V source.

The cable shield from each cable (pin10, 11, 12, 13 of the bilingual connector) is directly connected to chassis ground. The Twisted-Pair A Reference Ground must also be tied to signal ground through a combination of resistor and capacitor. The combination of a 1-MΩ resistor and 0.1-μF capacitor placed next to each connector is suggested.

The drivers on each port (TPA and TPB) are designed to work with an external 112-Ω termination-resistor network. This is to match the 110-Ω cable impedance. One network must be provided at each end of the twisted-pair cable. On bilingual ports, the midpoint of the TPA resistor network is directly connected to TPBIAS, a 1-μF capacitor for stability and a 270-pF capacitor for EMI on TPBIAS. The midpoint of the TPB resistor network is coupled to ground through a parallel RC network. These 112-Ω termination-resistor networks should be placed as close as possible to the PHY, and the common mode components should be placed as close as possible to the 112-Ω termination network.

Physical Layer Device – TSB41BA3

The electrical connection for TSB41BA3 is shown on sheet 2 and sheet 3 of the 1394a Link/TSB41BA3 schematic (Appendix A).

The power pins (DVDD-3.3, AVDD-3.3, DVDD(CORE), and PLLVDD(CORE)) of the TSB41BA3 must be grouped separately, and then decoupled to the GND pins through several high-frequency decoupling capacitors. The following rules apply to the decoupling capacitors:

Place one 0.001-μF capacitor as close as possible to each power pin. If two or more power pins are adjacent, only one 0.001-μF capacitor is required for the group.

Place one 0.1-μF capacitor as close as possible to each single power pin on the PHY. A single power pin is one that is not adjacent to another power pin.

TSB41BA3 requires an external 49.152-MHz crystal clock to generate a reference clock. The external clock drivers an internal phase-locked loop (PLL), which generates the required reference signal. This reference signal provides the clock signals that control transmission of the outbound encoded information. A 49.152-MHz clock signal is supplied to the associated LLC for synchronization of the two devices and is used for resynchronization of the received data when operating the PHY-link interface in compliance with the IEEE 1394a-2000 standard (BMODE input low). A 98.304-MHz clock signal is supplied to the associated LLC for synchronization of the two devices when operating the PHY-link interface in compliance with the IEEE 1394b-2002 standard (BMODE input high).

Crystal Selection: To ensure that the PHY oscillator starts under all operational conditions, TI recommends using a fundamental parallel mode crystal with a C_L of 20-pF or less with an ESR of 30-Ω or less. The termination capacitor values that should be placed on each leg of the crystal can be calculated with the following equation:

$C_{termination} = (C_L - C_{board}) \times 2$

Where:

C_{board} = (Board trace capacitance + PHY input capacitance)

If a 20-pF crystal is placed close to the PHY, then $C_{board} \cong$ 4-pF and $C_{termination} \cong$ 33-pF.

When a 1394 port is not brought out to a connector, it must be terminated correctly. The preferred method is to configure the port in the 1394a mode. In the 1394a mode, the TPB+ and TPB- pins must be tied together and connected to ground. The TPBIAS can be tied to ground through a 1-μF capacitor or left unconnected. The TPA+ and TPA- pins can be left unconnected. Port 2 in the schematic illustrates a properly terminated 1394a port.

The CPS pin detects the presence of cable power and is connected to the cable power through a 400-kΩ resistor. A common resistor value of 390-kΩ may be used. The node should always have the CPS pin connected to cable power through a 400-kΩ resistor, even if the PHY does not use cable power. If cable power is not available, the CPS may be tied directly to PHY ground.

The assertion of the /RESET pin resets the internal logic. An internal pull-up to VDD is provided so only an external delay capacitor is required for proper power-up operation. A 0.22-μF is the recommend value for the external delay capacitor.

The R0 and R1 terminals set the internal operating currents and the cable driver output current. To meet the IEEE 1394-1995 standard output voltage limits, a 6.34-kΩ ± 1% resistance is required.

S2_PC0, S1_PC1, and S0_PC2 are power class and ports mode configuration pins. On hardware reset, those pins, along with the other three mode configuration pins (S5_LINKON, S4, and S3), allow the user to configure the three ports of TSB41BA3. After the hardware reset, they become the power class pins. The power class pins program the power class value into the PWR field of the transmitted self-ID packet. This allows other nodes on the bus to understand the power requirements of the node. These pins are programmed according to the Power Class Description in the IEEE 1394a standard, Table 7-3. The schematic is programmed to a power class of “100” or decimal 4. This indicates that the node:

a) May be powered from the bus
b) Is capable of repeating power
c) Is using up to 3 W
d) Needs no additional power to enable the link

The power class pins are hard-wired to their values shown on the schematic.

S4 and S3 are configuration pins. Along with the other four mode configuration pins (S5_LINKON, S2_PC0, S1_PC1, and S0_PC2), they allow the user to configure the three ports of TSB41BA3. In this case, mode #22 is used for ports configuration, S4 is tied to the GND through a 1-kΩ resistor and S3 is tied to DVDD(3.3) through a 1-kΩ resistor.

VREG_PD is the enable pin for the internal voltage regulator that supplies the core voltage. For a single 3.3-V supply operation, this pin must be tied low to enable the voltage regulator. If this pin is tied high, then the core voltage must be supplied externally to the PLLVDD(CORE) and DVDD(CORE) respectively.

In the 1394b mode, TSB41BA3 uses the PINT to send status and interrupt information to the link. In the 1394a mode, the PINT can be left open and unconnected.

In the 1394a mode, the LCLK should be tied to ground.

TESTM, SE, and SM terminals are test control pins for manufacturing test. For normal operation, TESTM must be tied to DVDD(3.3) through a 1-kΩ resistor. SE and SM must be tied to ground directly.

PHY-Link Interface

The PHY-link interface of the TSB41BA3 can follow either the 1394a protocol or the 1394b protocol. When using any 1394-1995 or 1394a links such as the TSB12LV01B or the TSB12LV32, the PHY-link interface has to be in the 1394a protocol. In this case, the BMODE pin has to be tied low to GND. When using any 1394b link such as the TSB82AA2, the PHY-link interface has to be in the 1394b protocol. In this case, the BMODE pin is tied high. The BMODE pin only sets the mode of operation of the PHY-link interface; it does not set the mode of operation of the cable interface. No isolation is implemented in this schematic. The PHY and link operate off of the same ground plane.

To reduce EMI emissions and reduce reflections on the PCLK line, a series-damping resistor is recommended. The schematic shows a 0-Ω resistor, which is essentially a placeholder on the board. To reduce EMI, a 22-Ω resistor on the PCLK line is recommended. This resistor should be placed as close to the PHY as possible. Its value can be adjusted to reduce emissions. By slowing down the edge rates on PCLK, this 22-Ω resistor significantly reduces reflections that may occur when the distance between the PHY and link is large (greater than 4 inches in this case).

The Link Request signal (LREQ) is input to the PHY from the link. The link uses this to initiate a service request to the PHY. When the BMODE pin is deasserted, the IEEE 1394b-2002 BOSS arbitration is disabled and the LREQ request stream follows the 1394a specification.

CTL0 and CTL1 are bi-directional signals used to control the communication between the PHY and the link. These signals should be directly connected between the PHY and link. The CTL encoding follows the 1394a specification.

TSB12LV01B and TSB12LV32 are 400-Mbps link layer devices that use all data I/O lines (D0-D7) to communicate with the PHY. When status information is received from the PHY, only D0 and D1 are used.

S5_LINKON of TSB41BA3 is used both as a link-on output and as a configuration pin for the ports. On hardware reset, this terminal, along with other 5 configuration pins (S4, S3, S2_PC0, S1_PC1, and S0_PC2), allows the user to configure the TSB41BA3 ports. After hardware reset, this terminal is the link-on output, which notifies the LLC or other power-up logic to power up and become active. This terminal can be connected to the link-on input terminal of the LLC through a 1-kΩ resistor if the link-on input is available on the link layer.

If a power down option control for PD is not implemented, the PD pin on the PHY (pin 77) should be tied to ground through a 1-kΩ resistor to keep the PHY enabled.

Link-Layer Controller-TSB12LV01B

The TSB12LV01B is a 400-Mbps general-purpose IEEE 1394-1995 link-layer controller. The TSB12LV01B was intended for use in PC peripherals and telecom. It can transfer data between a host controller, 1394 PHY-Link interface, and external devices connected to the local bus interface.

The TSB12LV01B follows the big-endian architecture. Bit 0 is the most significant bit. Byte 0 is the most significant byte.

ADDR0 – ADDR7 is the 8-bit host address bus. This bus should be connected to the host processor address bus. All internal memory space (CFR and FIFO) may be addressed with only 6 of the 8 address lines. Address lines 6 and 7 should be grounded. Most significant byte of the TSB12LV01B address should be connected to the most significant byte of the host processor address bus, regardless of the host processor endianess.

The 32-bit host interface of the TSB12LV01B was designed to support a Motorola 68K-type microcontroller/microprocessor. The interface supports three access modes: normal, quick, and burst.

DATA0 –DATA31 is the 32-bit host data bus. This bus should be connected to the host processor I/O data bus. Most significant byte of the TSB12LV01B data bus should be connected to the most significant byte of the host processor data bus, regardless of the host processor endianess.

The BCLK is the clock input to the TSB12LV01B and should be tied to the host output clock. The TSB12LV01B can support clock rates up to 50-MHz.

The /CA pin of the TSB12LV01B is the active-low Cycle Acknowledge pin. It is a control signal to the host bus. When asserted, it signals an acknowledge from the TSB12LV01B to the host access cycle. It indicates that the access to the TSB12LV01B configuration register (CFR) space or FIFO is complete[1].

The /CS pin of the TSB12LV01B is the active-low Cycle Start pin that indicates the beginning of an access to the TSB12LV01B configuration or FIFO space[2].

/INT is an active-low Interrupt pin that should be connected to the Interrupt pin of the host. When /INT is low, TSB12LV01B notifies the host bus that an interrupt has occurred.

/WR is the Read/Write enable pin that should be connected to the WR pin of the host. When /CS is low and /WR is high, a read from the TSB12VL01B is requested by the host bus controller. To request a write access, /WR and /CS must be low.

[1] If interfacing directly to a Motorola 68K-type microcontroller/microprocessor, the /CA pin should be connected to the transfer acknowledge (/TA) pin of the processor.
[2] If interfacing directly to a Motorola 68K-type microcontroller/microprocessor, the /CS pin should be connected to the transfer start (/TS) pin of the processor.

The /RESET is the asynchronous system reset to the TSB12LV01B. This pin may be connected to the PHY reset pin, may be controlled by the host controller, or may be controlled via an external reset source.

The CYCLEIN input terminal is an optional external 8-kHz clock input that can be used to set up the isochronous cycle clock. This terminal is tied to VCC since it is not used in this case.

The CYCLEOUT output terminal is the TSB12LV01B version of the cycle clock. It is based on the timer controls and received cycle-start messages. It may be left open.

GPO0, GPO1, and GPO2 are general-purpose output bits. The power up default function for these terminals is GRFEMP, CYCDE, and CYST respectively if they are not being used. After power-up, these terminals may be programmed as general-purpose output pins.

Link-Layer Controller-TSB12LV32 (GP2Lynx)

The TSB12LV32 is a 400-Mbps IEEE 1394a general-purpose link-layer controller. The 12LV32 can be used in PC peripherals, such as printers, scanners, and desktop cameras. It can transfer data between a host controller, 1394 PHY-Link interface, and external devices connected to the data mover port (DMA interface).

The TSB12LV32 DIRECT pin is sampled during hardware reset to determine if galvanic isolation is present. If the terminal is high, no isolation is present. If the terminal is low, TI bus-holder isolation is used. The TSB12LV32 does not support Annex J isolation.

The CONTNDR terminal on the link defaults to being input on hardware reset. In the schematic, CONTNDR is tied to ground through a 1-kΩ resistor. This tells the link that the node is not contender for Isochronous Resource Manager (IRM) or Bus Manager functions. However, after power-on, the value of this pin may be driven internally from the CTNDRSTAT bit inside the link layer controller.

The TSB12LV32 has a programmable microcontroller interface with 8-bit or 16-bit data bus, five different modes of operation include burst mode, and a clock frequency up to 50-MHz. In this schematic, it is set up to operate in 16-bit fixed-timing mode with a Motorola 68000-style processor. To configure the TSB12LV32 for this mode, the MCMODE/SIZ1 and M8BIT/SIZ0 pins are tied to ground. Because the device is not configured for the Motorola ColdFire mode, the ColdFire terminal is also tied to ground.

The /MCS (Cycle Start) terminal is an active-low input terminal to the GP2Lynx. It signals the beginning of a microcontroller access to the GP2Lynx. The /MCS is connected to the TSZ line on the Motorola 68000. The /MCA (Cycle Acknowledge) is an active-low output signal representing the cycle acknowledge sent from the GP2Lynx to the TAZ terminal on the 68000. The /MWR is the read/write indicator. When asserted high, this input terminal indicates a read access from the GP2Lynx. When asserted low, it indicates a write access to the GP2Lynx. All data transfers on the microcontroller interface are synchronized with the rising edge of the BCLK.

The GP2Lynx device follows the big-endian architecture: to configure the micro interface for little-endian mode, the LENDIAN pin must be set high. In little-endian mode, the MD [0:15] lines are byte-swapped before it is written into the device's internal FIFO or configuration register (CFR). In the schematic, big-endian mode is used; therefore, LENDIAN is tied to ground. Because the Motorola 68000 processor uses bit 15 as the MSB (most significant bit) and the GP2Lynx uses bit 0 as the MSB, the data interface is swapped between the two devices (i.e., bit 15 on the GP2Lynx is connected to the bit 0 of the 68000). The micro interface can also be configured for data-invariant or address-invariant modes using the MDINV and MCMODE/SIZ0 terminals. However, MDINV is meaningful only when LENDIAN is enabled (high).

All GP2Lynx internal registers are 32-bit wide. However, since the Motorola 68000 processor operates on word boundary accesses, the GP2Lynx internally stacks 2 word writes before transferring tem to the link registers. No external byte stacking is needed.

Accessing all GP2Lynx internal registers requires only 7 bits of address lines. Since MA [0] is the MSB bit on the TSB12LV32, it is connected to A [6] of the 68000 processor. Consequently, MA [6] is connected to A [0] of the 68000 processor.

The /TEA terminal is connected to the Motorola TEAZ input terminal. This signal indicates the presence of an error in the data transfer operation.

The STAT0 – STAT2 are general status output terminals. These pins can be independently programmed to show one of fourteen possible internal hardware statuses. For more information on the programming of the STAT0 – STAT2, please refer to the latest TSB12LV32 data manual (TI Literature Number SLLS336B).

The CYCLEIN input terminal is an optional external 8-kHz clock that can be used to set up the isochronous cycle clock. This terminal is tied to VDD since it is not used in this case.

/INT is an active-low output terminal representing the logical NOR of all internal interrupts.

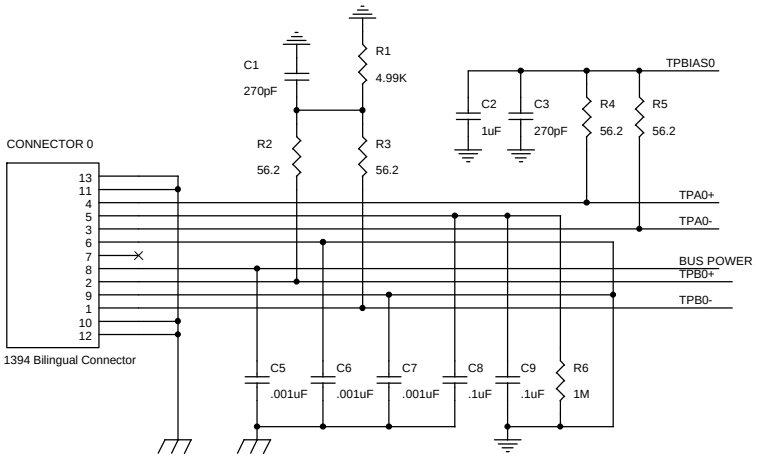
The data mover (DM) port is an 8/16-bit high-speed port that supports isochronous, asynchronous, and asynchronous streaming transmit/receive from an unbuffered port at 25-MHz. It is meant to handle an external memory interface of large data packets. The DM port has eight modes of operation and can support four-channels for isochronous transmit.

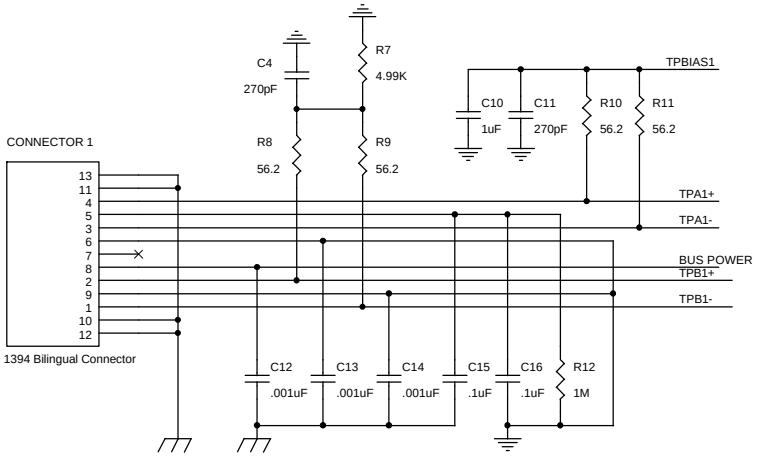
The DM port has seven control pins. For more information on the functionality of these pins, please refer to the latest TSB12LV32 data manual (TI Literature Number SLLS336B).

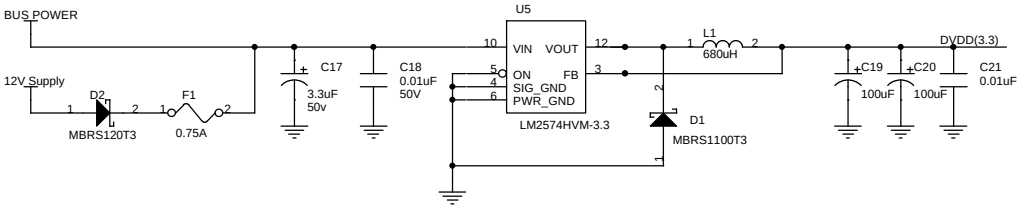
References

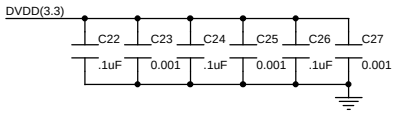
1. TSB12LV01B, IEEE 1394-1995 High-Speed Serial-Bus Link-Layer Controller (SLLS435A)
2. TSB12LV32, TSB12LV32I, IEEE 1394-1995 and P1394a Compliant General-Purpose Link-Layer Controller for Computer Peripherals and Consumer Audio/Video Electronics (SLLS336B)
3. TSB41BA3, IEEE 1394b Three-Port Cable Transceiver/Arbiter (SLLS155)
4. IEEE Std 1394-1995, IEEE Standard for a High Performance Serial Bus
5. IEEE Std 1394a-2000, IEEE Standard for a High Performance Serial Bus – Amendment 1
6. IEEE Std 1394b, IEEE Standard for a High Performance Serial Bus – Amendment 2

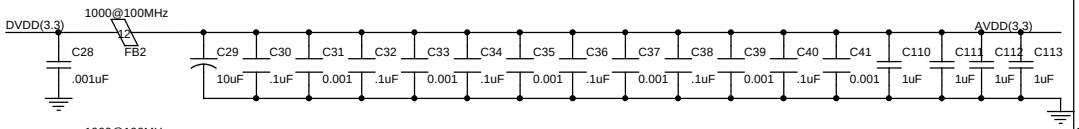
Appendix A. Reference Schematic

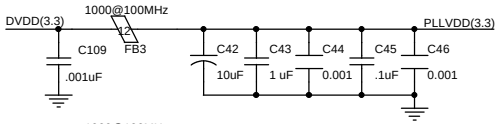


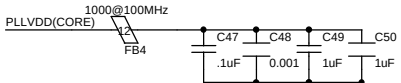


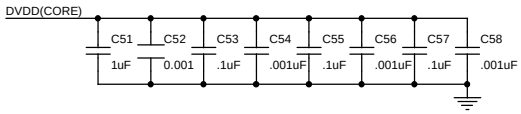












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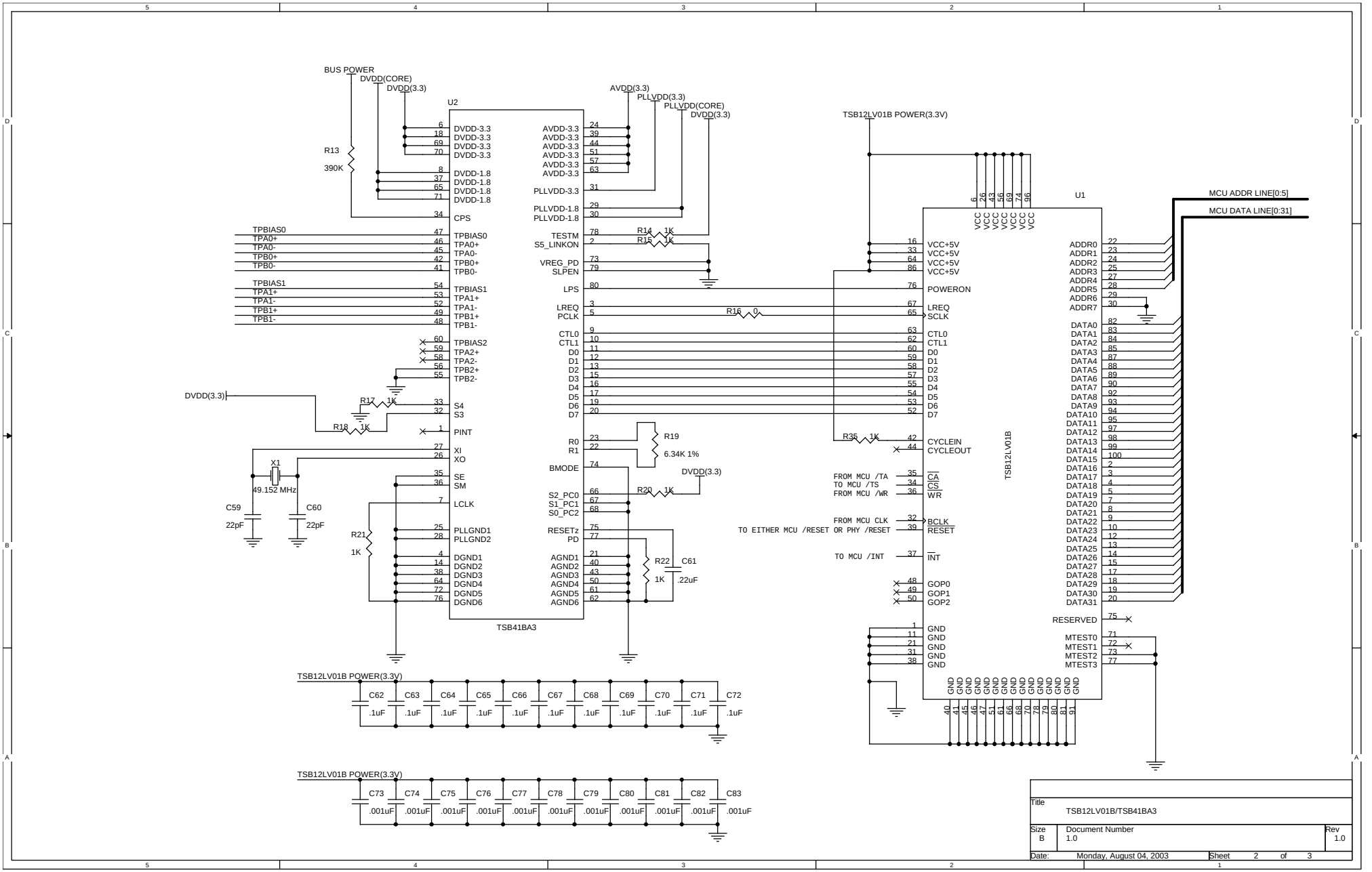
BUS POWER
DVDD(CORE)
DVDD(3.3)
U2
R13
390K
DVDD-3.3
DVDD-1.8
CPS
AVDD(3.3)
PLLVDD(3.3)
PLLVDD(CORE)
AVDD-3.3
PLLVDD-3.3
PLLVDD-1.8
TESTM
S5_LINKON
VREG_PD
SLPEN
LPS
LREQ
PCLK
CTL0
CTL1
D0
D1
D2
D3
D4
D5
D6
D7
R14 1K
R15 1K
TPBIAS0
TPA0+
TPA0-
TPB0+
TPB0-
TPBIAS1
TPA1+
TPA1-
TPB1+
TPB1-
TPBIAS2
TPA2+
TPA2-
TPB2+
TPB2-
S4
S3
PINT
XI
XO
SE
SM
LCLK
PLLGND1
PLLGND2
DGND1
DGND2
DGND3
DGND4
DGND5
DGND6
AGND1
AGND2
AGND3
AGND4
AGND5
AGND6
R0
R1
R19
6.34K 1%
BMODE
S2_PC0
S1_PC1
S0_PC2
RESETz
PD
R20 1K
R22 1K
C61 .22uF
R17 1K
R18 1K
X1
49.152 MHz
C59 22pF
C60 22pF
R21 1K
TSB41BA3
TSB12LV01B POWER(3.3V)
U1
VCC+5V
POWERON
LREQ
SCLK
R16 0
CYCLEIN
CYCLEOUT
R35 1K
FROM MCU /TA
TO MCU /TS
FROM MCU /WR
CA
CS
WR
FROM MCU CLK
BCLK
TO EITHER MCU /RESET OR PHY /RESET
RESET
TO MCU /INT
INT
GOP0
GOP1
GOP2
RESERVED
MTEST0
MTEST1
MTEST2
MTEST3
GND
TSB12LV01B
MCU ADDR LINE[0:5]
MCU DATA LINE[0:31]
ADDR0
ADDR1
ADDR2
ADDR3
ADDR4
ADDR5
ADDR6
ADDR7
DATA0
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7
DATA8
DATA9
DATA10
DATA11
DATA12
DATA13
DATA14
DATA15
DATA16
DATA17
DATA18
DATA19
DATA20
DATA21
DATA22
DATA23
DATA24
DATA25
DATA26
DATA27
DATA28
DATA29
DATA30
DATA31
C62 .1uF
C63 .1uF
C64 .1uF
C65 .1uF
C66 .1uF
C67 .1uF
C68 .1uF
C69 .1uF
C70 .1uF
C71 .1uF
C72 .1uF
C73 .001uF
C74 .001uF
C75 .001uF
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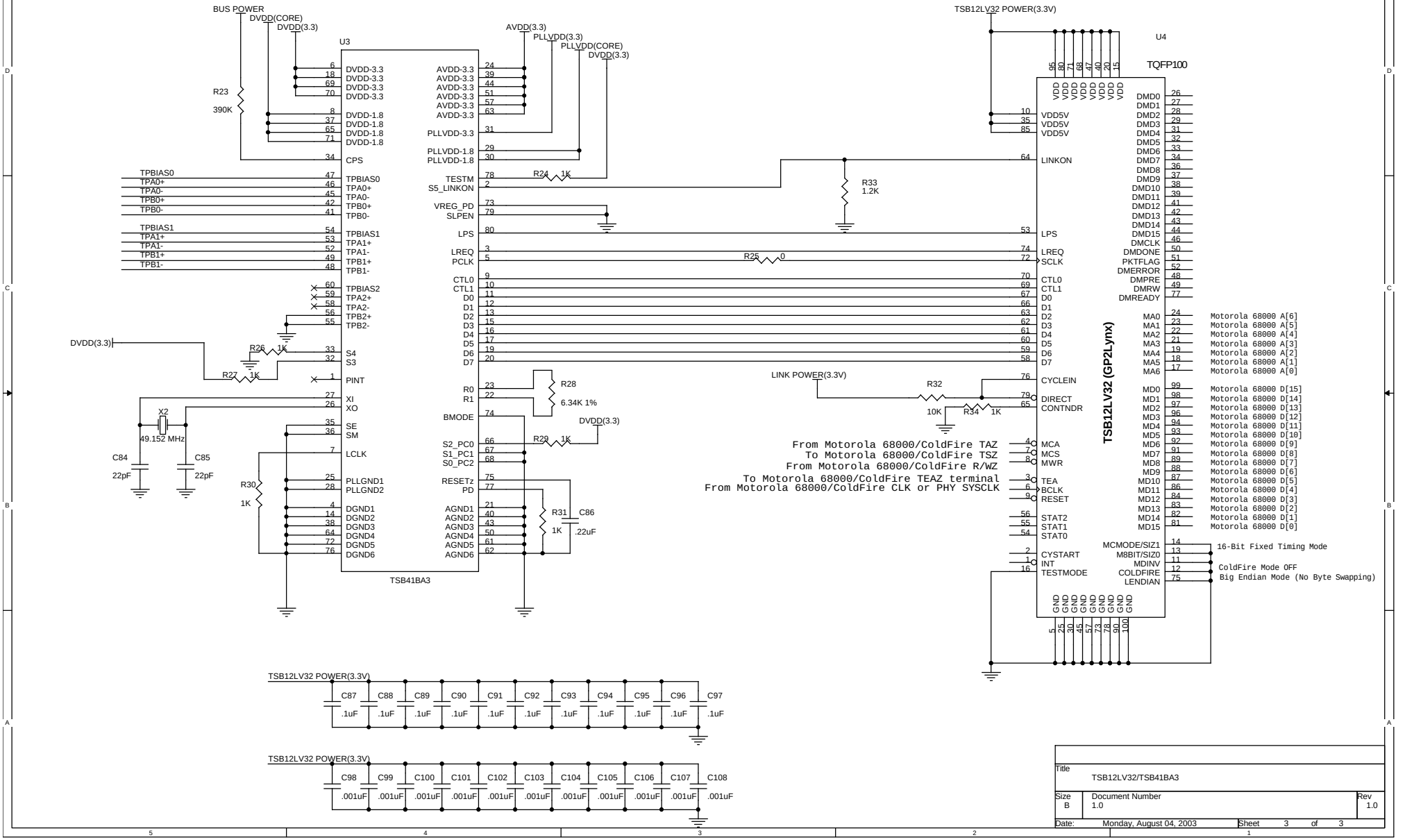

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