

# ***Recommendations for PHY Layout***

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## **Abstract**

This document makes recommendations for the layout of the PHY and Link layer devices in an IEEE 1394 environment. The optimal performance of an IEEE 1394 bus can depend on good board layout. An IEEE 1394 board that does not adhere to good layout guidelines may be susceptible to noise and interference, which could diminish the signal integrity. This document is not meant to be a general tutorial on good printed circuit board (PCB) layout practice; it is meant to highlight those areas of a 1394 node that may need special attention due to the special requirements of IEEE 1394 nodes.

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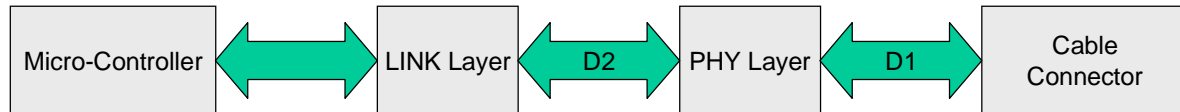
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## Introduction

Figure 1. A Typical IEEE 1394 Node



The Physical Layer (PHY) provides the digital logic and analog transceiver functions needed to implement a one- or multiple-port physical layer in an IEEE 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission.

The 1394 link layer communicates with the physical layer, packetizes the data decoded by the physical layer, provides cycle timing functions, and communicates the packets to and from the node controller. Figure 1 illustrates the logical layout points discussed in this document. Distance D1 between the physical layer and the cable connector and distance D2 between the link layer and the physical layer are discussed in this document. The layout for the distance between the micro-controller and link layer is heavily dependent on the microprocessor chosen and is outside the scope of this document.

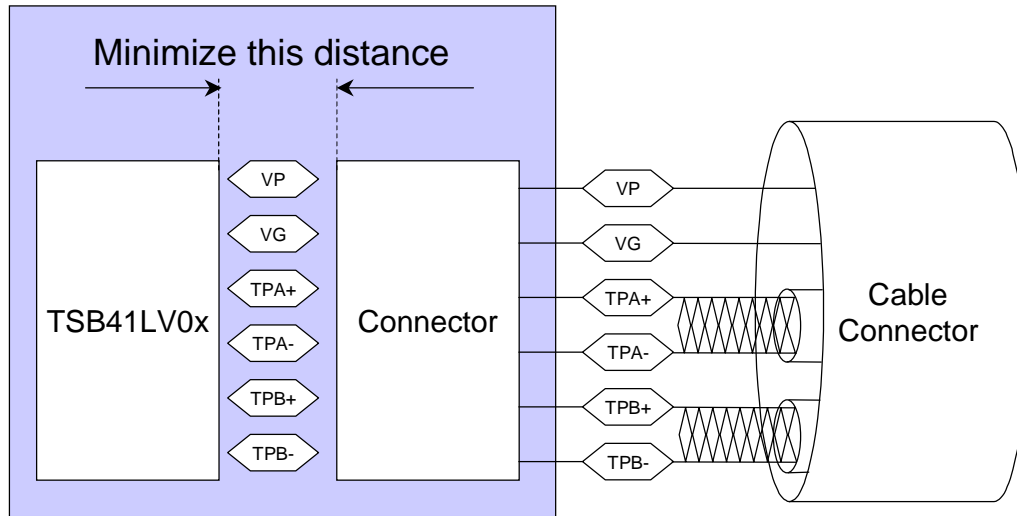
## Guidelines for Layout

This section discusses the following guidelines for layout:

- 1) The physical layer should be as close as possible to the 1394 connector (refer to Figure 1 and Figure 2). Because of the frequencies involved (up to 200 MHz at 400 Mbps) the etches propagating the differential twisted pair (TP) signal in a 1394 cable should be treated as transmission lines. The signal swing on the TP lines is relatively small (~110 mV), so any differential noise picked up on the twisted pair can affect the received signal.

When the twisted pair signal is propagated on etch without any shielding, the etch tends to behave as an antenna and picks up noise generated by the surrounding components and the environment. To minimize the effect of this behavior as well as other artifacts documented below, minimize the distance the twisted pair signal must be propagated on etch. The shielding on a standard 1394 cable inhibits this sort of interference while the signal is propagated through the cable.

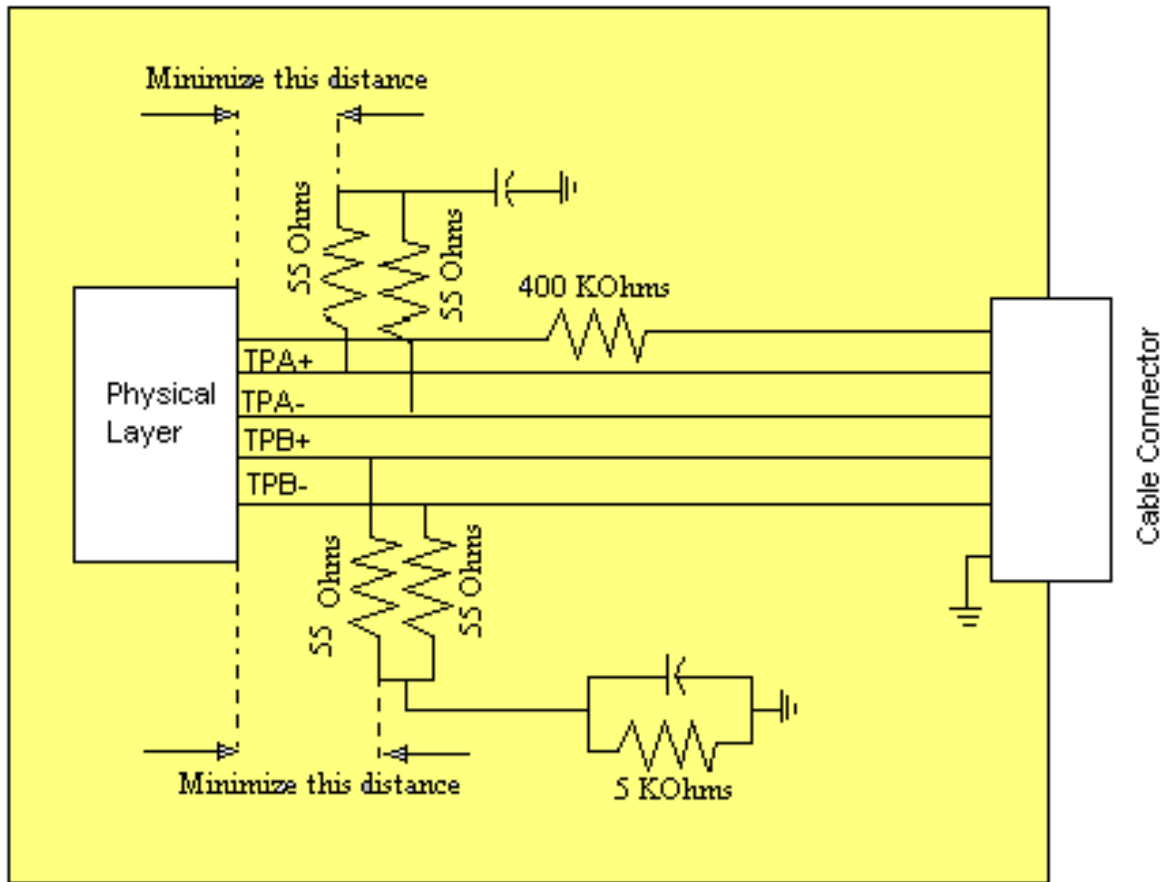
Figure 2. The PHY Connector and Cable Connector



- 2) Since the etch traces should be treated as transmission lines, they must match impedance with the cable and connector they are connected to. The IEEE standard 1394 twisted pair cable is specified to have a 110 ( $\pm 6$ ) ohms differential characteristic with a common mode characteristic impedance of 33 ( $\pm 6$ ) ohms (IEEE 1394-1995 paragraph 4.2.1.4.1). The input impedance of a node is also specified as 110 ( $\pm 1$ ) ohms in receive mode (IEEE 1394-1995 paragraph 4.2.2.5), hence the recommended termination network of 55 ( $\pm 1\%$ ) ohm resistors (for more information, see the TI *TSB41LV0x* data sheet).

To minimize reflections and maximize the power transmitted to the input pin, the etch length between the termination at the physical layer and the 1394 cable connector ports should be designed with a characteristic impedance of 110 ohms between the TP+ and TP- lines with a minimum of 33 ohms to ground. That is, the etch should have the same impedance as the cable and termination network. Having a different impedance causes reflections with less power being transmitted to the input terminals on the physical layer, which can reduce signal integrity.

Figure 3. Terminating Resistor



- 3) In a note related to #2, the termination resistors (55 ohms  $\pm 1\%$ ) should be located as close as possible to the TP (twisted pair) pins on the 1394 physical layer (refer to Figure 3). The purpose of the terminating resistor network is to match impedance with the cable transmission line, minimizing induced signal reflections. Placing the termination resistors close to the physical layer signal pin reduces the stub length between the physical layer terminal and the termination resistor. The longer the stub, the better the antenna it makes, and the more noise and interference it picks up that can distort the signal.

There are tradeoffs between these first three recommendations. The better the etch impedance matches the cable, the longer the TP etches can be—to a point. The lower the induced noise sources around the etches, the longer they can be—to a point. The better the impedance match of the etches, the longer the termination resistors can be from the physical layer—to a point. And the point it breaks will vary with all of the above factors (and more).

- 4) Rule of thumb for maximum etch length without matching impedance. We use the following justification to calculate the maximum length of etch on a PCB. After a signal has been transmitted, it travels the length of the etch and the reflection travels the equal length back, and all this must take place well under the rise time of the signal. If the rise time is longer, it behaves as a transmission line.

We use the following equation:

$L_{\text{etch}}$  = acceptable etch length

$D_{\text{max}}$  = max distance traveled during rise time

$S$  = propagation speed of signal

$C$  = speed of light

$L_{\text{etch}} < D_{\text{max}} / \sqrt{2\pi} \sim 2.5$ , or for a more conservative we use

$L_{\text{etch}} < D_{\text{max}} / 6$

$T_{\text{risetime}}$  = rise time

$D_{\text{max}} = T_{\text{risetime}} * S$

$S = C / \sqrt{E_r}$ ; propagation speed of signal

$C = 2.997 \times 10^8$  m/s

$E_r$  = Dielectric constant

Here is a conservative example of etch length without impedance match:

$L_{\text{etch}} = (T_{\text{risetime}} * S) / \text{divisor\_factor}$

Minimum 1394a Spec rise time = 0.5 ns

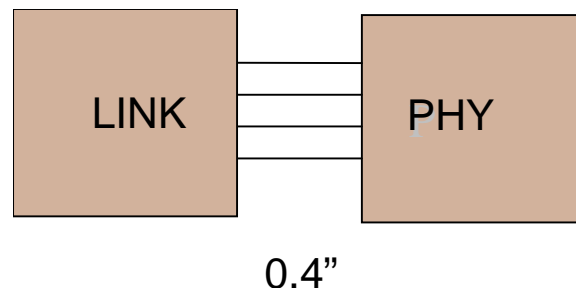
Maximum typical FR-4 dielectric constant = 5.3

Maximum divisor factor = 6

$L_{\text{etch}} = \{(0.5 \times 10^{-9} \text{ s})(2.997 \times 10^8 \text{ m/s}) / \sqrt{5.3}\} / 6$

$L_{\text{etch}} = 0.011$  meters (0.4")

Figure 4. Conservative Etch Length Between PHY-Link



Here is an unrealistic best-case example:

$L_{\text{etch}} = (T_{\text{risetime}} * S) / \text{divisor\_factor}$

Maximum 1394a Spec rise time (400 Mbps) = 1.2 ns

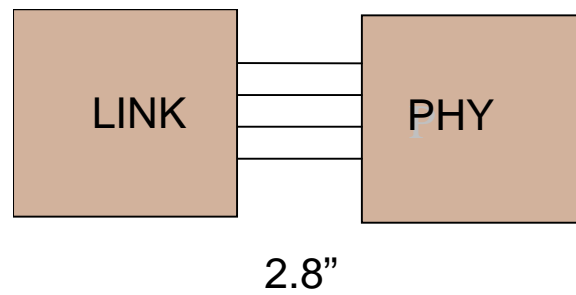
Minimum typical FR-4 dielectric constant = 4.1

Minimum divisor factor =  $\sqrt{2\pi} = 2.51$

$L_{\text{etch}} = \{(1.2 \times 10^{-9} \text{ s})(2.997 \times 10^8 \text{ m/s}) / \sqrt{4.1}\} / 2.51$

$L_{\text{etch}} = 0.071$  meters (2.8")

Figure 5. Best-Case Etch Length Between PHY-Link



- 5) The length of an etch depends on the rising edge of the signal. The longer the etch, the greater the chances for the signal to reflect back and behave as a transmission line.

Figure 6. Signal Traveling Over Long Etch

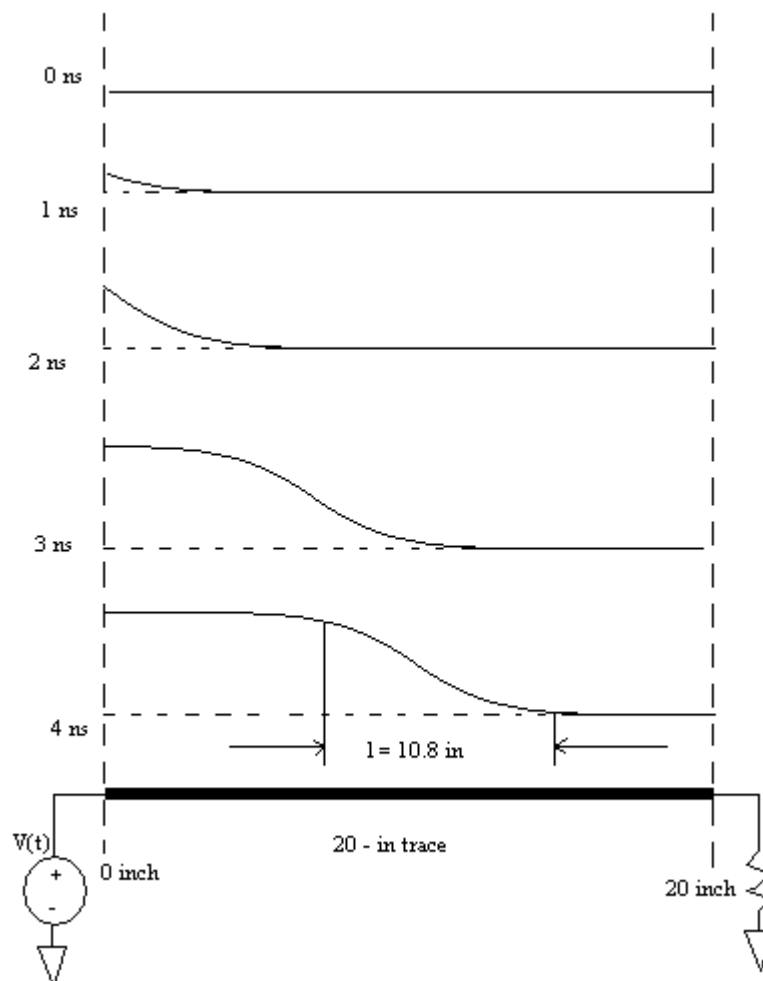


Figure 6 depicts a signal traveling over the length of an etch 20 inches long. At time 0 ns, there is no activity on the bus, and we see a flatline. At 1 ns, we see the start of the rising edge of the signal. By the time it is 3 ns, we see the complete signal that has been launched. When looking at the signal at 3 ns from the 0 inch of the etch, we see a logic 1, or a high. When looking at the same signal at the same instant from the other end of the 20-inch etch, we see a logic '0', or a low.

At time 4 ns, we see the same signal that was at 3 ns with no change except that it is traveling horizontally over the etch. This is an instant when the signal leading-edge wave is distributed across the impedance of the 20-inch etch itself. In these cases, the etch path should be treated as a transmission line. After the signal is launched, it must travel over the impedance of the etch. This causes the signal to lose strength and integrity.

*Figure 7. Signal Traveling Over Short Etch*

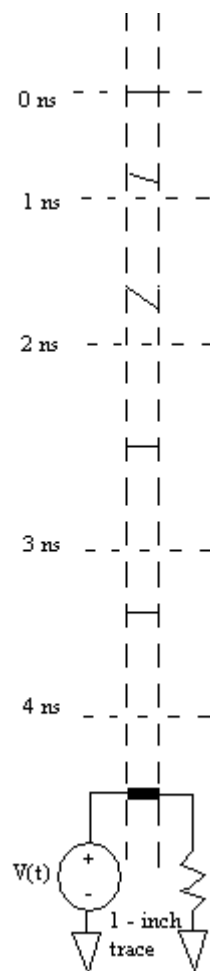
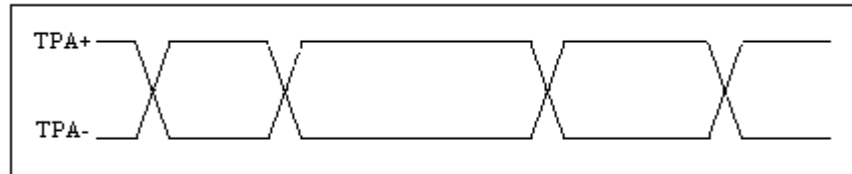


Figure 7 depicts the same signal as shown in Figure 6 but traveling over an etch length of 1 inch. At time 0 ns, there is no activity on the bus and we see a flatline. As time progresses, we observe that at no point do we see a logic high on one end of the etch while simultaneously seeing a logic low on the other end of the etch.

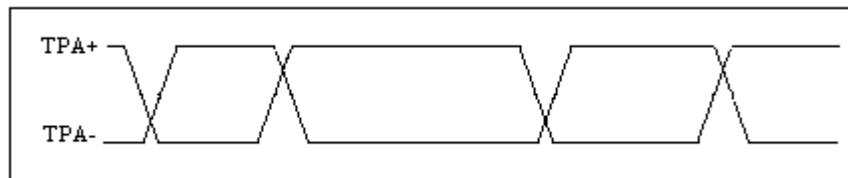
This indicates that the voltage on every part of the etch is uniform (almost) without any significant change in swing that would indicate a high on one end and a low on the other or vice versa.

In short length we do not see any transmission line effects take place and the signal integrity is maintained.

*Figure 8. The Etch Length for the Differential Signals Are Equal*



*Figure 9. The Etch Length of TPA- Is Longer Than TPA+*



*Figure 10. The Etch Length of Both Differential Signal Pairs Is Align Headed*

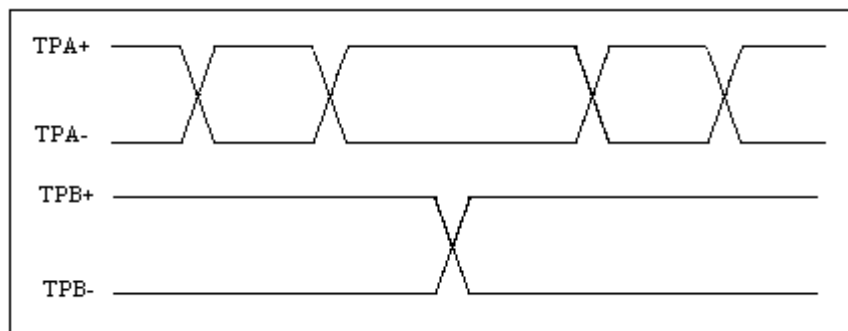
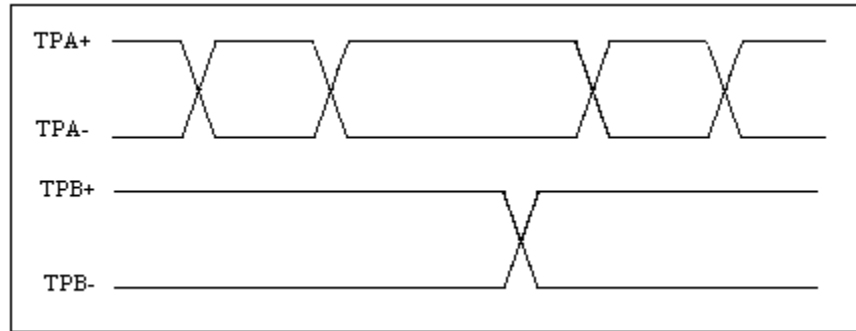




Figure 11. TPB Pair Etches Matched to Each Other but Longer Than TPA Pair

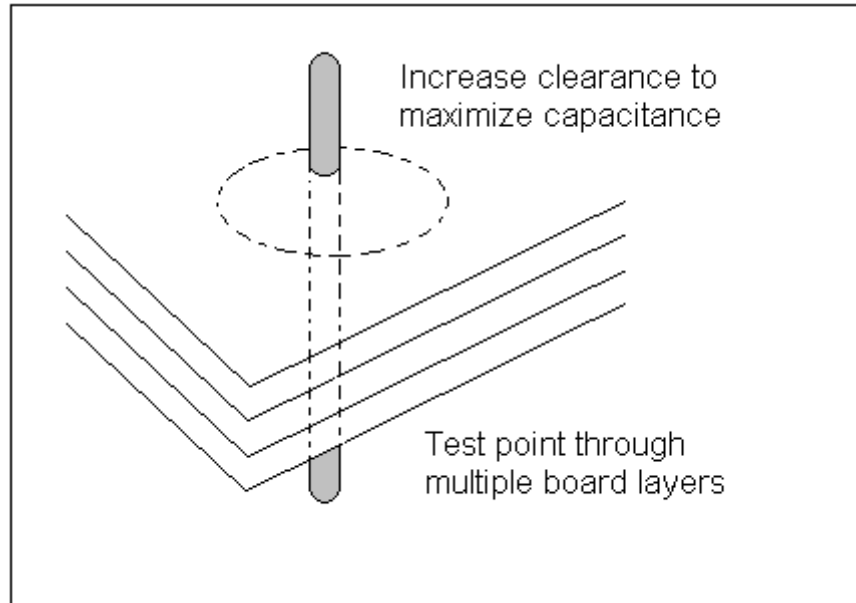


- 6) The etch lengths for the TPA+ and TPA- must be matched. For the same reasons, the TPB+ and TPB- etch lengths must be the same. In both cases this is required to reduce the skew in the differential signals (skew is measured by comparing the propagation delay on the two signals being measured).

The sensed difference between the TPx+ and TPx- signals is what is sensed at the receiver to determine a one or a zero. Any difference in length will change the timing relationship between the signals, reducing the skew margin built into the system, (see Figure 9 for an illustration). Also related to this, the TPA pair should have approximately the same etch length as the TPB pair for a single port.

The Data-Strobe encoding of the data being sent across the twisted pair depends on the relative timing between the “1”s and “0”s being signaled on the TPA and TPB differential pairs. If the delay of the signals through the etches is different, it will change the timing relationship of these signals, again reducing the skew margin of the coding. Therefore the etch lengths of the twisted pairs should be kept as close to the same as possible.

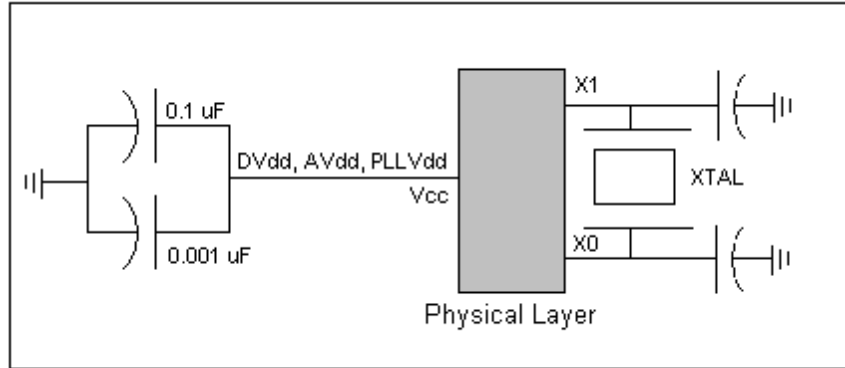
Figure 12. Vias Are More Likely to Pick Up Interference From Other Layers of the Board



- 7) Try to minimize the number of vias in the twisted pair lines. When a via must be used, try to increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. For similar reasons be careful using through-hole pins for test points on the twisted pair lines. Through-hole pins add inductance to the transmission line, which can reduce signal integrity.
- 8) Keep the 24.576-MHz crystal and its load capacitors as close as possible to the PHY pins x0 and x1. (Refer to Figure 13). The greater the distance the greater the chances of interference from noise that can interfere with the frequency lock of the internal phase locked loop (PLL). Maintaining the frequency is extremely crucial and critical to all of the applications. Components on the board that can interfere with the clock frequency should not be placed in close proximity to the clock. Frequencies from power sources or large capacitors can cause modulations within the clock or cause it to go out of sync. In these instances errors such as dropped packets occur.
- 9) The external crystal and internal oscillator drive the internal phase locked loop, which generates the required reference signal. The reference signal is internally divided to provide the clock signals used to control transmission of the outbound encoded Strobe and Data information and the system clock (SCLK) sent to the link layer to synchronize the PHY-Link interface.
- 10) The SCLK (clock generated by the PHY) must be within 100 ppm (pulse-position modulation) of 49.152 MHz. When designing an application with the 1394 Physical layer, the termination capacitor on each leg of the crystal, feeding XI/XO terminals of the PHY must be properly chosen to ensure reliable operation. If the capacitance used is too low, then the frequency accuracy at the SCLK terminal will be out of the 100-ppm specification. This can cause data errors on large packets. If the capacitance is too high, the oscillator will not oscillate. For optimal results the load capacitance of the crystal must be matched with the capacitor placed at the crystal

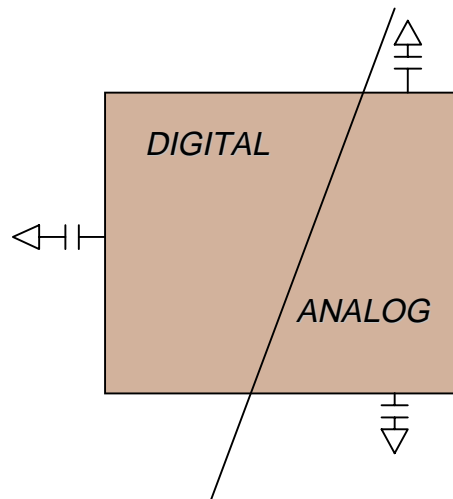
terminals. If adjacent nodes are more than 200 ppm with one another, long packets sent across the 1394 bus may be corrupt, with the final bits of the packet being lost.

Figure 13. Power Supply and Clock Connection to the Physical Layer



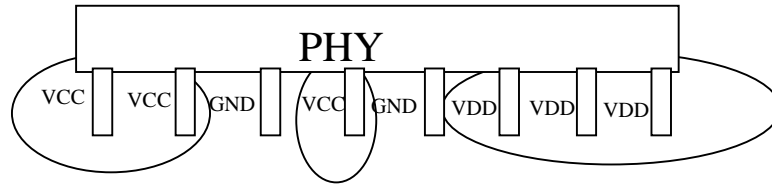
- 11) Place power decoupling capacitors as close as possible to the PHY power supply pins. The capacitors create a filter to reduce the noise coupled into the device across the power plane, which helps maintain signal integrity. Keeping the etch short between the capacitors and the device minimizes the stub antenna, minimizing the noise coupled in on the device side of the filter network. The noise is also very much dependent on the application, so we try to take all precautions and use a conservatively noisy environment for our example.

Figure 14. Top View of a 41LV0x PHY



- 12) There are two parts to the PHY, the analog and the digital. The analog pins are concentrated on one half of the PHY, and the digital pins are on the other half. For optimal performance we suggest having one 0.001- $\mu$ F cap for each power pin, i.e. VCC, VDD, and PLL. Also have a 0.1- $\mu$ F capacitor for each separate power group. A group is any number of power pins from 1 and higher that are adjacent to each other.

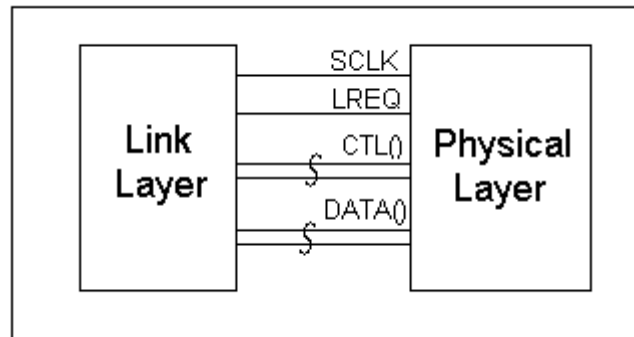
Figure 15. Power Pin Groups in a PHY



In Figure 15, there are three separate groups. The first group consists of two VCC pins adjacent to each other, the next group has one VCC pin, and the third group consists of three VDD pins together. In this scenario, we need one 0.1- $\mu$ F capacitor for each group.

- 13) When using a switching power regulator to produce the regulated PHY power from the unregulated cable power or from another higher voltage supply, it should be placed carefully. The switching regulator should be kept away from, specifically, the twisted pair etches, the external clock crystal (or clock oscillator if used), and the physical layer device in general. Switching regulators are a source of noise and, if placed close to sensitive areas on a circuit board, increase the chance of the noise being coupled into a sensitive signal.

Figure 16. The PHY/Link Interface Signals Should Be Close and Have the Same Etch Length



- 14) Try to keep the PHY-Link interface (SCLK, LREQ, CTL [0,1], and DATA [0:x]) short (less than 4 inches if practical). The signals driven across the PHY-Link interface are at 3.3-V CMOS levels (if both the Link and PHY are 3.3-V CMOS) but are at 49.152 MHz and should be treated with due care. These signals should also all be approximately the same length. (Refer to Figure 16). The short distance is to minimize noise coupling from other devices and signal loss due to resistance. They should be kept the same length to reduce propagation delay mismatches across this synchronous interface.



## EMI Interference

The significance of the electromagnetic compatibility (EMC) of electronic circuits and systems has led to more stringent requirements for the electromagnetic properties of equipment. The EMC of an electronic circuit is mainly determined by how components are laid out with respect to each other and by how electrical connections are made between components.

Every current flowing in a line generates a current of the same magnitude flowing in a corresponding return line. This loop creates an antenna that can radiate electromagnetic energy whose magnitude is determined by the current amplitude, repetition frequency of the signal, and the geometry of the current loops.

One strategy to reduce radiated EMI (electromagnetic interference) is to terminate the SCLK signal to ensure a clean clock signal. This may be done with an approximately 10-ohm to 20-ohm series resistor at the source (PHY) side of the SCLK signal to increase the source impedance and reduce reflections. The impedance value used will be a function of the characteristic impedance of your board. To minimize the change in delays on the PHY-Link interface, the same termination should also be placed on the data lines, the control lines, and the LREQ line.

Additionally, to reduce the EMI propagated through the cable shield, experiment with different values for the capacitors used in the parallel RC network to isolate the cable shield ground from chassis ground.

Additional recommendations to reduce EMI may be found in the TI application note *Printed Circuit Board Layout for Improved Electromagnetic Compatibility* at <http://www.ti.com/sc/docs/psheets/appnote.htm>.

- ☐ Ensure ground return paths are as close as possible to signal paths. Longer return paths create loops that are likely to radiate EMI.
- ☐ Series terminate SCLK to help clean up clock signal
- ☐ Avoid discontinuities in ground return paths.
- ☐ Isolated ground planes should be capacitively coupled together to provide a signal return path.
- ☐ Avoid running digital CMOS-level signals (SCLK) near sensitive analog signals (TP lines, Crystal) when running traces.
- ☐ Place resistor ACAP to the PHY. Resistor value is dependent on the characteristic impedance of the board. Series Resistor + Source Impedance  $\approx$  Etch Impedance
- ☐ To reduce EMI from the cable shield and noise coupled on to chassis ground, experiment with different value caps to isolate cable shield ground from chassis ground.
- ☐ Do not use 90-degree corner traces—this causes discontinuities.

## PowerPAD Packaging

The 400-Mbps PHY is housed in a high-performance, thermally-enhanced package. Use of the PowerPAD™ package does not require special consideration except to note that the PowerPAD, which is an exposed die pad in the bottom of the device, is a metallic thermal and electrical conductor. Therefore, if not implementing PowerPAD PCB features, the use of solder mask may be required to prevent any shorting by the exposed PowerPAD of connections, etches, or vias under the package. The recommended option is to not run any etches or signal vias under the package but have a grounded thermal land.

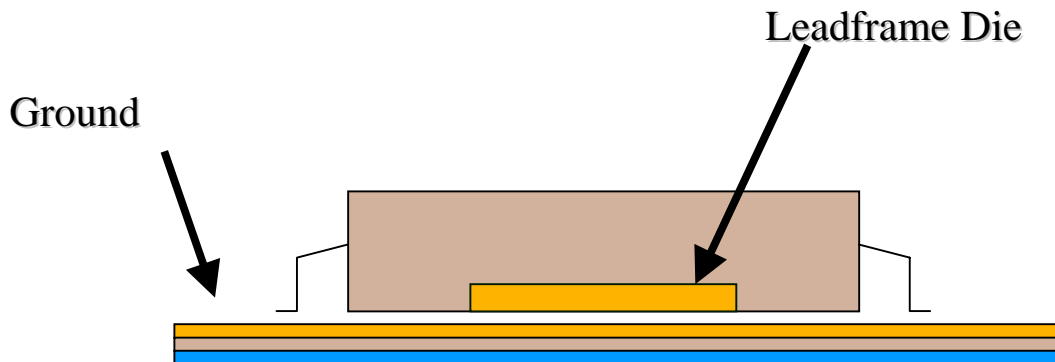
Figure 17. Bottom View of Different Packages



It is recommended that there be a thermal land, an area of solder-thinned-copper, underneath the PowerPAD package. The thermal land will vary in size depending on the PowerPAD package being used, the PCB construction, and the amount of heat that needs to be removed.

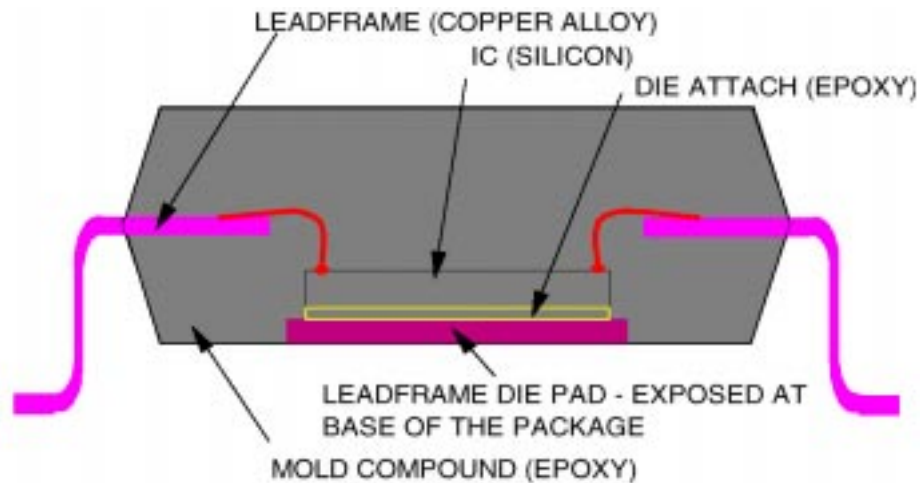
The thermal die pad at the bottom of the device is directly connected to the silicon die.

Figure 18. PowerPAD Package on a PCB Layout



Using the PowerPAD feature, we are not only able to improve thermal performance but also the electrical grounding of the device. It is also recommended that the device ground pin landing pads be connected directly to the grounded thermal land. The land size should be as large as possible without shorting device signal pins. The thermal may be soldered to the exposed PowerPAD using standard reflow soldering techniques. Using the PowerPAD packaging, we are able to get a Theta JA (junction to ambient) of 17.3, and a Theta JC (junction to case) of 0.12 at no additional cost.

*Figure 19. Section View of a PowerPAD Package*





## TI Contact Numbers

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### INTERNET

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